What is claimed is:

1. A placement and routing method for a clock distribution circuit which receives a clock and supplies the clock to a load circuit, said method comprising the steps of:

(a) temporarily placing and routing a group of elements having a common input capacitance to form said clock distribution circuit; and

(b) until an evaluated value of clock skew becomes equal to or smaller than a target value, making a selective replacement of an element belonging to said group of elements among a plurality of elements having a common input capacitance and selected from a group consisting of a plurality of driver elements having different driving capabilities, a driver element having an opened output pin and a capacitance element interposed between an input pin and a stable potential line.

2. The placement and routing method for a clock distribution circuit according to claim 1, wherein said step (b) makes the selective replacement of an element belonging to said ground of elements between a first driver element and a second driver element identical to said first driver element and having an opened output pin until said evaluated value of clock skew becomes equal to or smaller than said target value.

3. The placement and routing method for a clock distribution circuit according to claim 1, wherein said step (b) makes the selective replacement of an element belonging to said element group between a driver element and a capacitance element sharing a common input capacitance with said driver element and interposed between an input pin and a stable potential line until said evaluated value of clock skew becomes

equal to or smaller than said target value.

4. The placement and routing method for a clock distribution circuit according to claim 1, wherein said step (b) makes the selective replacement of an element belonging to said element group among a plurality of driver elements having different driving capabilities and a common input capacitance and having their input pins placed in equivalent positions and their output pins placed in equivalent positions until said evaluated value of clock skew becomes equal to or smaller than said target value.

5. A placement and routing method for a clock distribution circuit which receives a clock and supplies the clock to a load circuit, said method comprising the steps of:

(a) temporarily placing and routing a group of driver elements having their input pins placed in equivalent positions and their output pins placed in equivalent positions to form said clock distribution circuit; and

(b) until an evaluated value of clock skew becomes equal to or smaller than a target value, making a selective replacement of a driver element belonging to said group of driver elements among a plurality of driver elements having different driving capabilities and having their input pins placed in equivalent positions and their output pins placed in equivalent positions.

6. A method of manufacturing a clock distribution circuit which receives a clock and supplies the clock to a load circuit, said method comprising the steps of:

(A) performing a placement and routing of said clock distribution circuit comprising the steps of,

(A-1) temporarily placing and routing a group of elements having a common input capacitance to form said clock distribution circuit, and

(A-2) until an evaluated value of clock skew becomes equal to or smaller than a target value, making a selective replacement of an element belonging to said group of elements among a plurality of elements having a common input capacitance and selected from a group consisting of a plurality of driver elements having different driving capabilities, a driver element having an opened output pin and a capacitance element interposed between an input pin and a stable potential line; and

(B) fabricating said clock distribution circuit obtained through said step of placement and routing in a semiconductor substrate.